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Pete Singer

3D: A Whole World of Challenge

September 6, 2007

Major manufacturing challenges related to production on very thin wafers need to be overcome for 3D chip stacking to become a mainstream technology. That was the main message from Dr. Christo Bojkov, director of WLP engineering and technology at Maxim Integrated Products (Dallas, Tex.), speaking at the Semitool PEAKS Wafer Level Packaging Symposium. Bojkov is also involved with work at Texas A&M, working with Professor Manual Soriaga.

Bojkov said stress on thin wafers resulted in serious problems with warp and bow, as well as delamination, cracking, blistering -- problems compounded by a lack of metrology standards and tools. The thinner the wafer, the bigger the problem!

A common error, he said, is that stress measurements are typically done soon after various process steps, but the results are not meaningful because stress changes dramatically with time. This is well documented in an IBM article "Mechanism for Microstructure Evolution in Electroplated Copper Thin Films Near Room Temperature" that appeared in the Journal of Applied Physics. How much stress is acceptable? Bojkov said stay below 100 Mega Pascal and "you'll be happy."

Stress comes in two flavors: compressive and tensile (no film has zero stress says Bojkov) depending on factors such as crystal size and/or surface roughness, depending on the film composition. Compressive stress is more desirable, since tensile films "really peel off" – the problem is all films tend to stay tensile!

Subsurface damage is also a major problem that is not well understood. Presently, people use surface roughness measurements to get a handle on the degree of damage, but Bojkov said that was nonsense.

A big surprise was the Bojkov said that a carrier approach, where thinned wafers are temporarily bonded onto a thick carrier wafer, was "more forgiving" but that it was "highly unacceptable" in a manufacturing environment and that much work needed to be done to demonstrate that such a process was reliable. EVG and Brewer Science have developed a carrier process, and will have volume iron-man-type-test results available by the end of the year. The temporary bond can withstand process temperatures up to 220C and debonds at 250C. EVG presently offers a 200 mm tool, with a 300 mm version due out next year.

Yet another problem, said Bojkov is that wafers are always sitting on edge when transported, which can lead to chipping.

Wafers with TSVs are heavily perforated, "like swiss cheese" which creates additional problems.

Bojkov concluded with a list of challenges for the EMC3D consortium to address:

- How to prevent wafer-edge chipping without edge rounding on thinned wafers.
- How to safely back-grind thinned wafers and control subsurface damage.
- How to reduce intrinsic and thermal stress on metalized wafers.
- Understand thermal gradients in sandwiched wafers.
- Develop spec limits and control limits for stress measurements.

Posted by Pete Singer on September 6, 2007 | Comments (1)

Industries: Semiconductor Packaging, Wafer Processing

September 7, 2007
In response to: 3D: A Whole World of Challenge
Phil Garrou commented:

Pete, No one looking seriously at 3D Integration is contemplating handling the thin wafers on their produc tio lines. By thin I mean 50 microns or less which is what most of the proposed proceses are looking at. In all of these cases the wafers are either on a carrier wafer or are already bonded t the stack. In both of these cases stress needs to be managed, but is not a major issue. In terms of Fabs not supporting the use of carrier wafers - Fabs do not like any cange. Fabs were highly resistant to introducing Cu to their lines...but in the end...because it was necesary...they did.

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