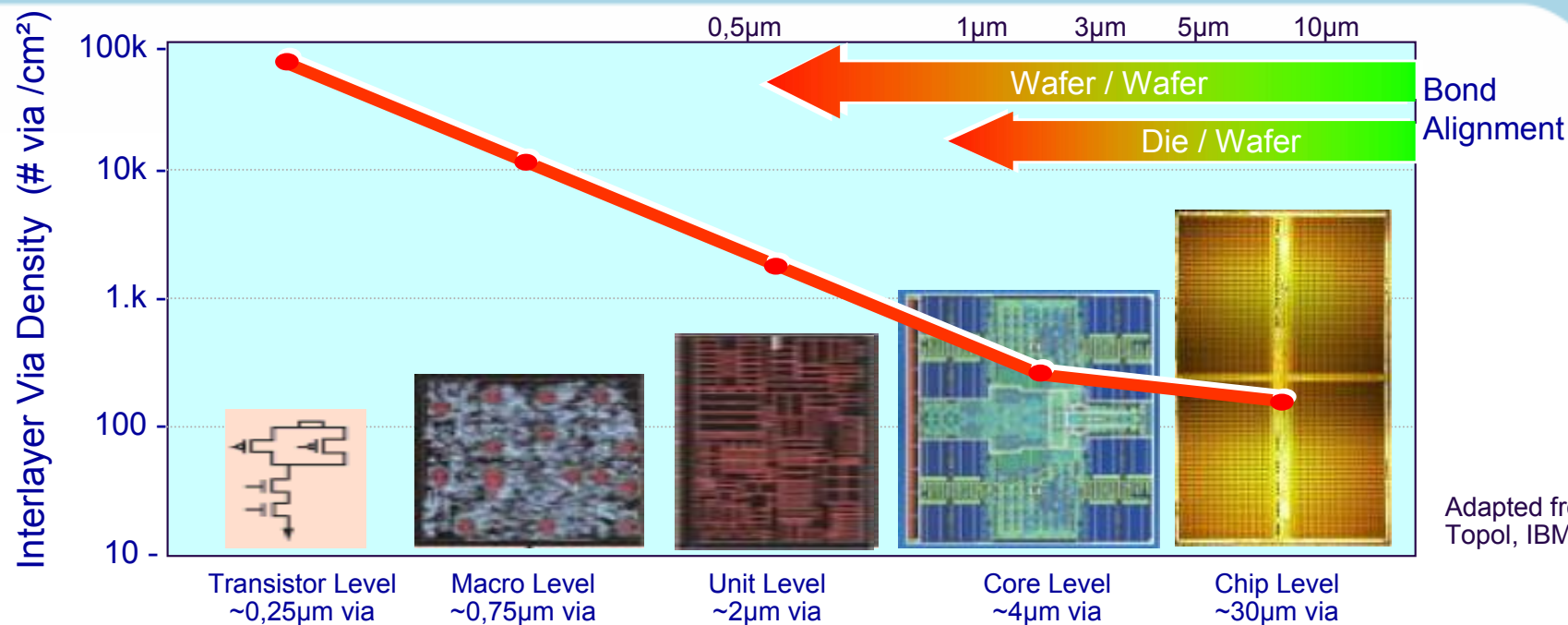


3D Integration by Thru-Silicon-Via Stacking Requirements and Trends

A view from memory

Symposium EMC3D
Munich, June 27th 2007

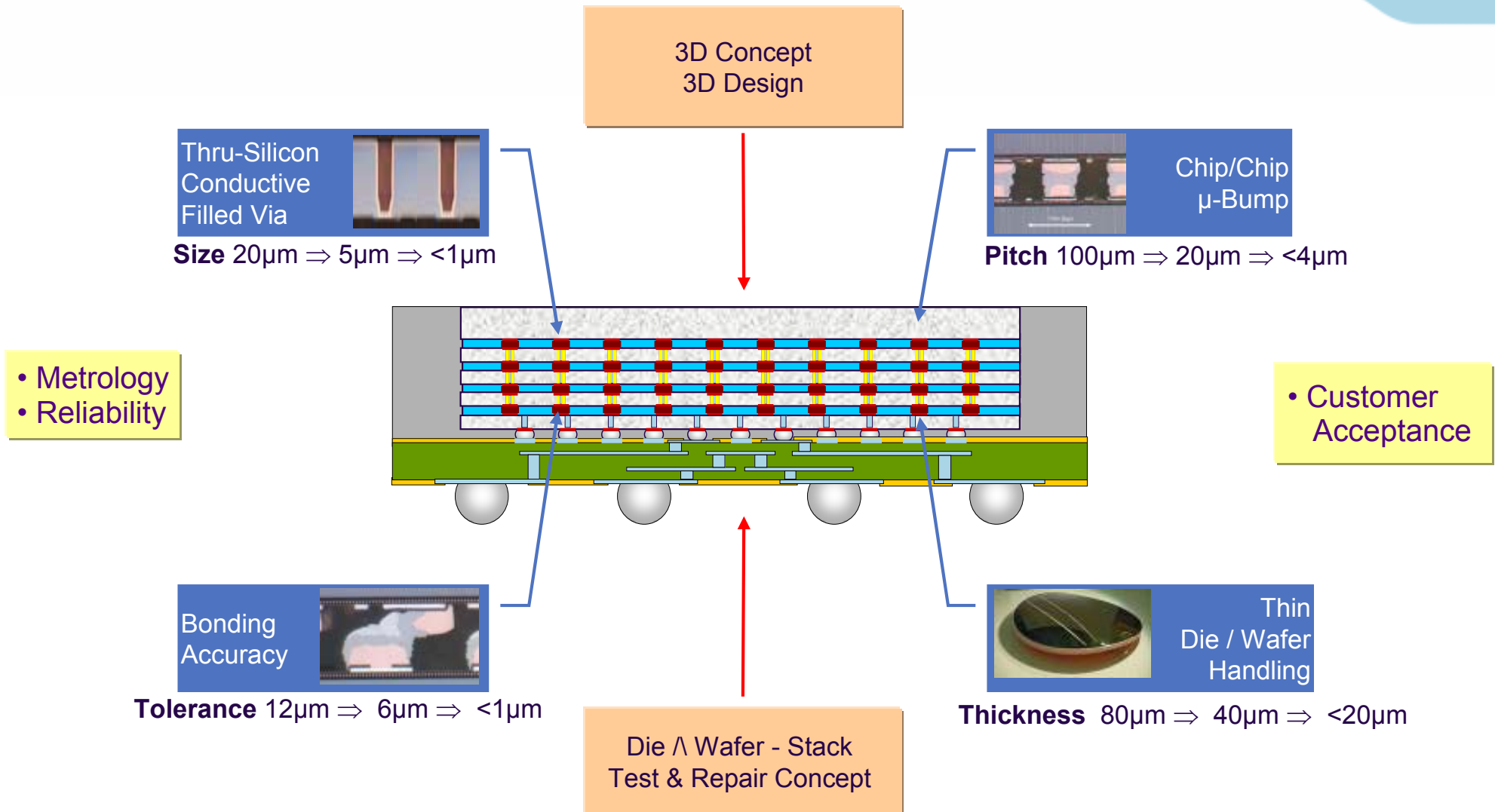
The introduction of Thru-Si-Stacking (TSV) into volume will be across Memory



Architecture	Via Size	Via Process	Chip/Via Connection	Stacking Type	1st Application	
Standard Chip Architecture	Large, (~ 20µm) ~ 10...100/chip	Post Front-End	On Chip RDL	Die / Die Die / Wafer	Flash	Phase 1
First 3D Elements	Medium, (< 5µm) ~ 200...1000/chip	Pre /In /Post Front-End	Integrated in Me layers	Die / Wafer Wafer / Wafer	DRAM, Sensors, Processor / Memory	Phase 2
Complete 3D Design	Fine, (< 1µm) ~ 1k...100k/chip	Pre /In Front-End	Integrated In Me layers	Wafer / Wafer	???	Phase 3

The 3D Thru-Si-Via Stacking Technology will be introduced stepwise to be beneficial

Key Elements for 3D TSV-Stacking

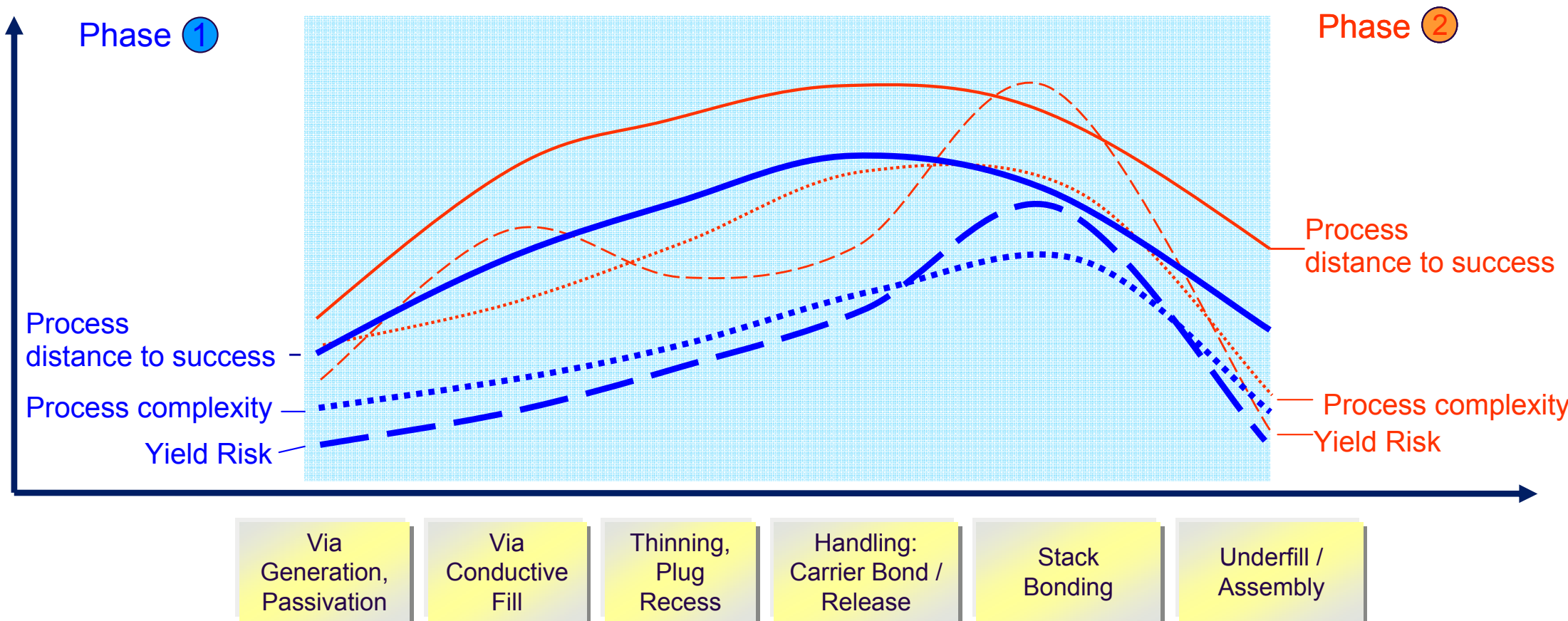


3D TSV stacking technology requires a combined strategy in realization of Design / FE-Processing / Test Strategies / BE-Processing adapted to product

Complexity, Risk of the Key Enabler Technologies



Example	Die Thickness	Via Diameter	Via Conductor	Interconnect	# of Layers	Underfill
Phase ①	60μm	30μm	Cu-RDL	SnAG Bump	4	liquid underfill
Phase ②	20μm	3μm	Cu-plug	Cu / Cu	6	underfill



The maturity and risk of the key enabler technologies is still different distributed → improvement !

Our Message to the Manufacturer Community



- We believe, that *our memories* will need a clearly defined TSV stacking flow that is *balanced* to our running FE & BE technology and to our products
- We believe, that a '*general technology*' or a '*general pilot line*' generated for '*all products*' will bring us *no benefit* in the short run
- But we welcome all equipment and material manufacturer to work with us and invite you to *visit us* at our Dresden development site
- To be successful our strategy is to work close with those manufacturer that fits best to our business

Thank you

**The World's Leading
Creative Memory Company**

