

High Throughput Low CoO Industrial Laser Drilling Tool

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Abstract

Recent advances in UV DPSS laser drilling of blind, micron sized vias in silicon (Si) are presented here highlighting some of the attractive features of this approach such as high throughput, excellent sidewall quality and depth uniformity. Drilling rates >2000 vias/s can be achieved for certain layouts through careful choice of laser parameters, utilisation of rapid optical galvanometers and optimisation of the micro-machining strategy. Since via drilling is a direct write process no lithography steps are required, enabling rapid setup times and significantly reduced cost. Resulting vias suffer no impairment in quality and issues such as the entrance lip and debris are mitigated, while a sidewall roughness of ~ 120 nm is obtained. Depth uniformity of $\pm 4\%$ is achieved over 300mm wafers and the taper angles of sidewalls approach the optimal 85° value for void free copper plating, eliminating the need for ion assistance during the PVD process. Wafers are not subjected to adverse temperature variations since little heat is absorbed into the wafer bulk during machining, as the heat affected zone surrounding via is less than $1\mu\text{m}$ and exhibits negligible induced stress, as shown by micro-Raman spectroscopy. Finally it is shown that the laser process is suitable for structured wafers comprising oxide layers and metal pads, and is compatible with active devices. Via diameters of $10\text{-}80\mu\text{m}$ are achievable in a percussion drilling regime, satisfying the majority of current requirements for industrial interconnect applications. Initial results for diameters of $5\mu\text{m}$ are also presented.

Key words: laser micromachining, percussion laser drilling, TSV, tapered silicon via, through silicon interconnects.

Introduction

Advances in lithography and packaging consistent with Moore's law are now placing even greater demands on existing packaging tools. Emerging from these demands is an exacting set of requirements that are not easily satisfied by existing tool capabilities and processes. In this paper it will be argued that Laser Micromachining [1] offers a viable alternative to the incumbent processes and that it will also meet the future demands of roadmaps for advanced packaging technology.

The laser micromachining approach can be divided into two main areas dicing/scribing [2] and via drilling [3-6]. This paper is primarily concerned with via drilling. Through Silicon Vias (TSV) are increasingly important in the semiconductor packaging industry to provide compact interconnects in 3D stacking applications [7]. Currently two technologies, Laser Drilling and Deep Reactive Ion Etching (DRIE), are employed to generate these vias and while each has certain benefits there is as yet no agreement on which provides the most effective solution.

During its early development laser via processes suffered from throughput and size limitations where typical drill rates were below 30 Vias/s and diameters exceeded $25\mu\text{m}$. Laser technology was then first directed towards applications with low density requirements such as CMOS sensors [4] and NAND flash memory [5]. Advances in laser via development and throughput will enable laser drilling for DRAM [6] in the short-term and likely for processors and logic - in the longer term.

Of the known laser drilling regimes of helical, trepanning and percussion, only the latter provides a significant throughput advantages over DRIE. In a percussion drilling regime a consecutive sequence of laser pulses are focused to the same point in a workpiece to drill a via of fixed depth and diameter. The number of laser pulses and the pulse energy dictate via depth, the beam size governs the via diameter while the overall drill rate is determined by the laser repetition rate and the speed at which individual vias can be addressed.

Recent advances in the process development of blind, micron sized vias drilled in Si by UV DPSS lasers exhibit a high throughput, clean top and an excellent sidewall quality along with a negligible heat affected zone.

Range of via sizes in percussion laser process

The range of via diameters routinely available in the percussion regime extends from 15 - 80 μm in a standard via drilling tool. Examples of the optimised laser process for via diameters of 15 μm , 30 μm , 50 μm and 80 μm with corresponding depth range is shown in Fig.1. Intermediate diameter ranges are accessible by utilising a variable beam expander, while smaller diameters <10 μm can be achieved (Fig.2) through the use of shorter focal length scan lenses. This range of sizes satisfies the majority of current requirements for industrial interconnect applications.

CoO and maintenance of Laser Drilling Tool

The laser drilling process is insensitive to via position on the wafer and thus via depth uniformity of $\pm 4\%$ is attained over full 300mm wafers. The depth uniformity is largely determined by the shot-to-shot laser energy stability and could reach $\pm 1\%$ (Fig.2). This compatibility of the laser via drilling process with 300mm wafers stands in contrast to existing difficulties which some DRIE approaches experience in maintaining uniformity and significantly reduces the cost of ownership (CoO) for large-volume industry.

Being maskless, the laser process eliminates the need for various expensive lithographic steps such as coating, exposure, development and photoresist stripping [4]. Via positions are programmed by CAD on the tool, enabling rapid setup times, product changeover and reduction of CoO. The laser process for TSV is flexible and can be utilised for both Front End and Back End machining allowing both “Via-first” and “Via-last” approaches to be adopted. In addition the bypassing of the mask laser process gives developers a rapid chip prototyping tool that enables them to iterate designs quickly from design modifications to machined wafer.

Finally, laser drilling tools have low cost consumables and low maintenance requirements comprising primarily factory supplied DI water for washing and pump diode replacements in the laser once every 2-3 years (>20,000 hours of average lifetime).

Material removal rates in laser ablation

Dual pulse lasers have been shown by Forsman *et al.* to enhance Si removal rates to $\sim 4\mu\text{m}/\text{shot}$ with optimised temporal separation between the dual pulses [8] while silicon ablation rates in excess $\sim 20\mu\text{m}/\text{shot}$ have been attributed to laser-induced explosive boiling with secondary plasma heating [9]. However, violent ejection of large $\sim 2\text{-}10\mu\text{m}$ micro-droplets by phase explosion forms unwanted debris [10] and bubble nucleation causes a degradation of the via sidewall quality as well as $\sim 20\%$ depth variation [11].

For the first time it is reported here that material removal rates exceeding 20 μm per single laser shot, and which do not impair the sidewall and entrance quality of resulting via, are experimentally observed (Fig.3) Fluence, spatial beam quality and shape, focusing geometry, pulse shape, duration and repetition rate have all been optimised to achieve this result.

Throughput of laser drilling tool

Material removal rates reported are coupled with very high drill rates of up to 2000-2500vias/s for certain via dimensions and densities (Fig.4). Unlike DRIE which is a parallel process, the laser process proceeds sequentially where typically individual vias are completed prior to subsequent vias being processed. Rapid movement between vias is achieved using optical galvanometers and the laser process is extremely fast within their scanning field which may cover one or several dies. Movement between scanning fields or die groups is performed by linear stages resulting in a step-and-scan approach.

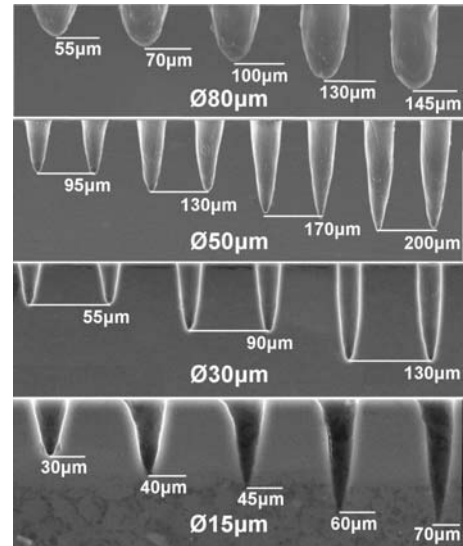


Fig.1 SEM image: range of via diameters and depth machined on laser drilling tool.

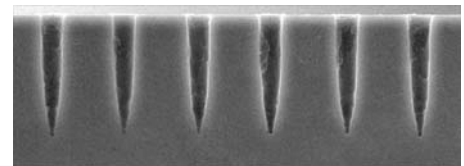


Fig.2 SEM image: cross-sectioned line of 10 μm diameter vias with $\pm 0.8\%$ depth variation.

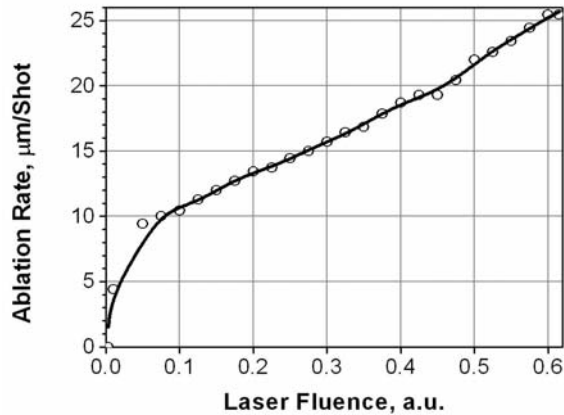


Fig.3 Single-shot ablation rate of monocrystalline Si wafers versus incident laser fluence at 355nm wavelength.

Consequently, drill rates for a particular device depend both on the die size and the via density. Drill rates for the X300V-Ultra production tool vary for the different products from, for example, 17,000Vias/min for a 300mm wafer comprising 657 dies with 100 vias per die of 20µm diameter and 60µm depth up to >53,000Vias/min for a similar wafer with 1000 vias of 15µm diameter and 50µm depth per die, 657,000 vias per wafer. Corresponding throughput is rated at 15 wafers/hour for the first example cited and 4-5 wafers/hour for the latter.

Besides greater ablation efficiency, available with current UV laser systems, the high drilling rates have been facilitated by the progress in the development of rapid scanning galvanometers providing reduced settling times at the higher jump speeds used to move between vias. Further advances are anticipated in the product roadmap which will enhance the throughput by >50% within the next 2-4 years.

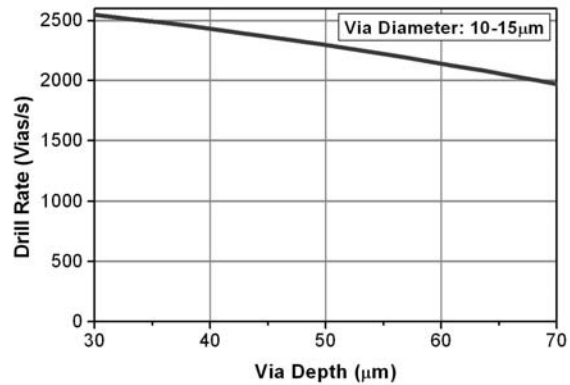
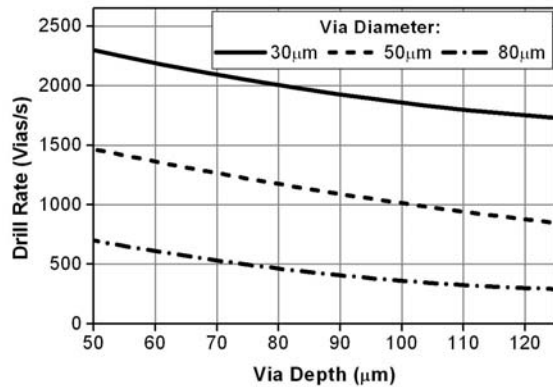


Fig.4 Drill rates within scan field for 30-80µm and 10-15µm diameter Via range.

Sidewall quality at high ablation rates

Sidewall quality is widely regarded as being crucial for TSV interconnects applications to permit efficient and effective metallization. Any imperfections can potentially occlude regions of the sidewall during the coating process resulting in a defective via with adhesion and/or continuity issues. Certain DRIE processes suffer from such an artefact where sharp, regular scallops, produced due to the interplay of mask-etch steps in a narrow closed channel like a via, give rise of inter-via electrical leakage current [12] and increase the risk of dielectric breakdown.

The optimised laser process developed at Xsil ensures smooth sidewalls on silicon wafers. From the examples of Fig.5 it can be seen that smooth via sidewalls are obtained that enable straightforward metallization. Surface roughness figures of ~0.12µm have been measured using a Zygo White Light Interferometer on vias which were processed at removal rates as high as ~20µm/shot. This roughness value is associated only with occasional large scale irregularities of condensed Si while fine structure is not visible optically giving the surface a polished appearance.

Optimal taper angles for via metallization

Physical Vapour Deposition (PVD) is a low temperature technique adopted for barrier and seed layer deposition used to both insulate via sidewalls prior to metallization and promote adhesion during and subsequent to metallization. However, the technique does not appear to be suited to the via sidewalls which are typically produced by DRIE processes where scalloping seems to be currently inherent in processes with acceptable throughput. Alternative techniques, such as Chemical Vapour Deposition (CVD), tend to produce vias whose metalized

interconnects suffer from weak adhesion to the sidewall and which results in low yield subsequent to wire bonding. High aspect ratio vias with straight sidewalls are also a challenge for conformal sputtering and void-free electroplating. Ion assisted PVD is an expensive solution to address this problem.

It is known that a tapered via ensures conformal seed and simplifies Cu-filling by reducing the effective aspect ratio [13]. A tapered via profile is therefore preferred over the vertical for barrier, seed layer deposition and rapid plating [13]. The form-factor does not suffer since the bottom diameter remains unchanged and an insignificant fraction of interconnects densities are sacrificed. The restrictions imposed by the DRIE process do not easily lend themselves to resolving the taper and scalloping issue which are inherent in certain DRIE processes without adversely affecting the throughput [12]. This is especially so in cases where attempts are made to maintain uniformity of via depth and quality over 300mm wafers. Attempts to compensate for the inherent difficulties have had only limited success, yielding vias with tapers limited to a few degrees that tend to straighten at relatively small aspect ratios. Dual-etch techniques, employed to address the problem of tapered sidewalls with Bosch DRIE by subsequent isotropic etch [12], also smooth the scallops.

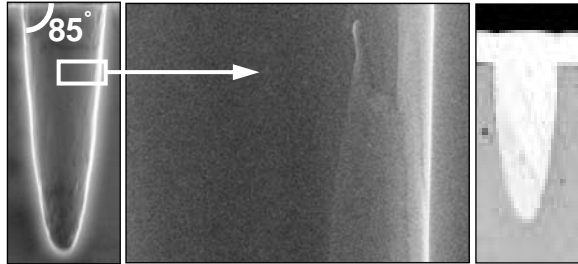


Fig.5 Cross-sectioned via of 30 μ m diameter by SEM: sidewalls tapered at optimal 85° angle (left), close-up (centre) and Cu-metallized (right).

In contrast to the DRIE approach to via generation the laser process reported here enables rapid machining of high quality vias with sidewalls tapered at optimal 85° angles, considerably simplifying and accelerating metallization. Taper angles of laser processed vias such as those displayed in Fig.5, approach the optimal value for void-free Cu-plating and can, in turn, eliminate the need for ion assistance during the PVD process. These properties alone make laser drilled vias attractive for any TSV interconnect application.

Incorporated cleaning process

The laser process being a form of drilling unavoidably produces particulate matter which results from the subsequent condensation of material ablated by the laser. It is necessary to carefully deal with this material which can adhere to the wafer surface in the vicinity of the via. In certain configurations and setups a lip or raised rim which extends for a few microns around laser drilled vias results. An optimised laser process eliminates the lip surrounding vias by utilising the higher efficiency of plume ejection by recoil pressure while a vacuum fume extraction arm collects ejected particles during micromachining reducing the incidence and degree of potential contamination.

To satisfy the most demanding clean room requirements an efficient cleaning process is incorporated into production tools, eliminating residual Si debris (Fig.6). A built-in washing station, comprising an integrated spin-coater allows wafers to have a water soluble sacrificial layer deposited on them prior to laser machining which is then washed off subsequent to machining. Any debris produced during the laser drilling process that is not captured by the vacuum system is trapped on the sacrificial layer and also removed during the wash process. Figure 6 illustrates the appearance of typical wafers before and after wash.

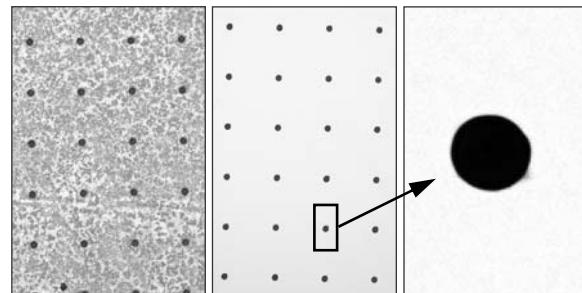


Fig.6 Optical microscope images of debris on protective coating after laser drilling (left), coating with debris washed (centre) and resulting via close-up (right).

Induced Stress and Heat Affected Zone (HAZ)

Induced stress impacts on yield, rendering devices more susceptible to fracture during packaging processes, while the Heat Affected Zone (HAZ) dictates the interconnect density and hence defines the device form factor. A substantial HAZ is thought to exist when machining with Q-switched lasers. Induced stress exceeding 1GPa has been observed by Amer *et al.* [14]. However, HAZ is significantly minimized in optimised laser process described here. Induced stress and HAZ of cross-sectioned via samples have been measured by Micro-Raman Spectroscopy on

a Renishaw®-1000 system coupled to a CCD camera and a Leica optical microscope. Single-spot Raman spectra were recorded from different areas of the sample in a backscattering geometry with an Ar⁺ ion laser at 514nm and 457nm wavelength used as an excitation source (Fig.7). All peaks observed had a symmetrical shape and could be fitted with a single Lorentzian function. The LO Si-Si phonon peak for unstressed Si is located at 520cm⁻¹. Under the compressive stress this peak is shifted to the higher frequency side, while for tensile stress - to the low-frequency side. Induced stress was calculated from these shifts and scanning was performed in the area of maximal expected stress within 7 microns of the sidewall as shown in Fig.7.

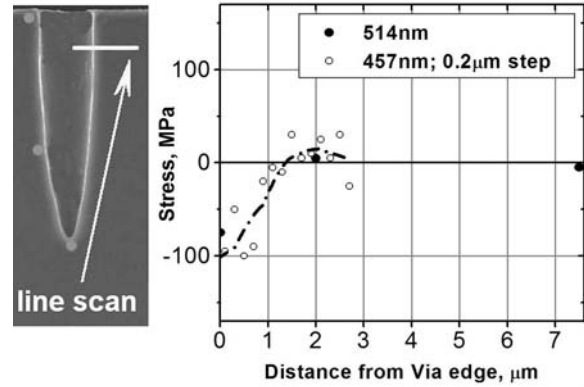


Fig.7 Single-spot micro-Raman measurements (left) and stress scan (right).

The results of the analysis demonstrate that the degree of induced stress is low attaining a maximum value of 100MPa and rapidly relaxes within 1μm of the via sidewall. This analysis suggests that the wafers being drilled do not suffer adverse temperature variations, that little heat is absorbed into the wafer bulk and that the heat affected zone surrounding the vias is less than 1μm, and as such exhibits negligible induced stress. No amorphous Si layer was detected. Stress-relief at high fluences may be associated with annealing mechanism by plasma heating [14]. It is known that magnetically enhanced dense plasma causes physical and latent device damage in RIE reaction chamber. Laser drilling does not cause charging and is safe for devices.

Preliminary results for 5μm diameter via

Via diameters ranging from 10-80μm are covered in a rapid percussion drilling regime by tuning the optical set-up in a standard via drilling tool. R&D work is currently ongoing for vias of 4-6μm diameter addressing targeted roadmaps of DRAM [15] and logic [16] manufacturers till 2012.

The main impediment to attaining large via diameters is imposed by the maximum pulse energy available from industrial UV high repetition rate Q-switched DPSS lasers. Therefore, via diameters >80μm are machined on the same tool in trepanning regime with a consequent loss of throughput. However, large vias in Silicon are not of significant interest for interconnect applications.

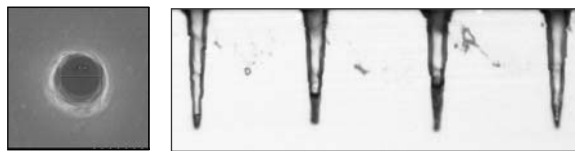


Fig.8 Via of ~5μm diameter laser drilled in Si: top view (left) and cross-section (right).

Nevertheless, optimisation of opto-mechanical design allows via diameters as small 4-6μm to be achieved at the speeds approaching 3000Vias/s (Fig.8) while maintaining an optimal sidewall taper angle of 85°. Restrictions for smaller via diameters are also imposed by wavelength-related diffraction limit and spatial quality of laser beam. Nevertheless, substantial diameters reduction <2-3μm is envisioned by precise control of instantaneous power with ps lasers and other emerging techniques [17].

Limitations for small diameter vias arise from opto-mechanical restrictions: spherical aberrations in commercially available scan lenses, inevitable trade-off between focal length, separation between the scanning mirrors in galvanometer and its aperture; maintenance considerations: hazard of scan lens contamination by ejected plume and effective throughput reduction with smaller scan field; strict requirements for the chuck flatness.

Backside wafer drilling. Machining through metal

Laser process is less selective than DRIE to a diversity of microelectronics materials and is suitable even for patterned and structured wafers comprising oxide and nitride layers, Al, Ni, Ti and Cu pads (Fig.9), unpolished contaminated surfaces (Fig.10) and even epoxy compounds.

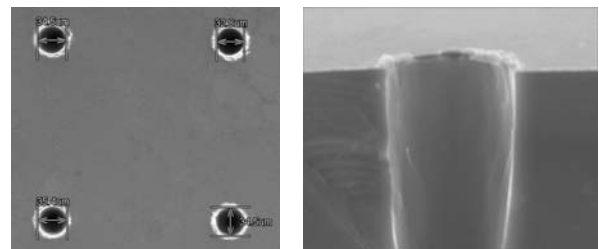


Fig.9 SEM images of vias machined through the copper pad.

Metals are more susceptible to thermal damage in laser ablation than Si due to higher thermal conductivity. Nevertheless overburden becomes critical only for thickness of metal layer $> \sim 1\text{-}2\mu\text{m}$. Rapid progress shown recently in commercialisation of DPSS and fibre lasers of ps and sub-ps pulsewidth permits suppression of residual overburden by reduction of thermal diffusion length. Reliability of short pulse width lasers is now increasingly approaching that of standard industrial Q-switched lasers.

Sometimes via etching on the back grinded side of Si wafer is needed while polished surface is attached to another substrate. However, particles and contaminations on rough Si substrate create problems for DRIE such as plasma arcing in reaction chamber. In contrast laser process demonstrates a good quality (Fig.10).

Conclusions

Laser via machining is an enabling technology for front and back end TSV interconnect applications providing reduced cost of ownership (CoO), by eliminating the requirement for expensive photolithography steps, increasing throughput, and a platform for simplified seed deposition and accelerated electroplating. It has also been shown to be a stress-free process, safe for active devices, having reliable operation and inexpensive maintenance. Laser drilling aims to reduce fabrication costs by bypassing expensive wafer fabrication process such as photolithography, RIE, CVD and IPVD.

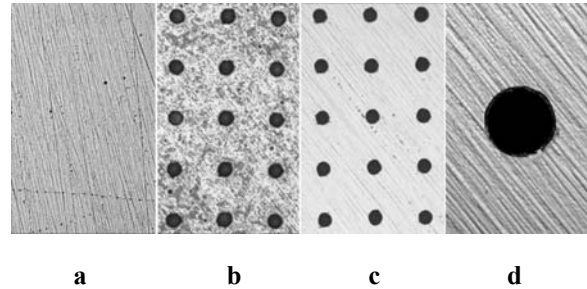


Fig.10 Unpolished wafer by optical microscope - a, debris on protective coating after machining – b, coating and debris washed – c, resulting via close-up – d.

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