



Contacts:

EMC-3D

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Brewer Science, Inc., joins EMC-3D consortium to develop cost-effective 3D Thru-Silicon-Via interconnects

Equipment and materials provider joins EMC-3D international consortium of equipment providers, materials companies and researchers to address complex integration of Thru-Silicon-Via (TSV) 3D chip interconnects.

May 1st, 2007. Brewer Science joins the international consortium EMC-3D, dedicated to providing cost-effective integrated Thru-Silicon-Via (TSV) technology for chip stacking applications.

EMC-3D, a semiconductor 3-D equipment and materials consortium, is addressing the technical and economic issues of creating 3-D interconnects using TSV technology for chip stacking and advanced MEMS/sensors packaging. Through collaboration with research partners, the consortium will develop processes for creating micro-vias between 5 and 30 μm on thinned 50- μm 200- and 300-mm wafers using both via-first and via-last techniques. The primary goals of the consortium are to create a robust process flow at a cost of less than \$200USD per wafer.

Brewer Science provides a diverse product portfolio of material and equipment solutions to the semiconductor, optoelectronic, MEMS, and packaging industries. Its product lines include specialty materials for use in litho, wafer thinning, wafer etching and bulk micromachining applications, including a wafer bonding material for thin wafer handling processes; organic bottom anti-reflective coatings (BARC's) tailored for a wide range of applications under the ARC® brand of products; an enabling proprietary wafer edge

wrap protection process; spin-coat/develop/bake equipment; benchtop processing equipment; and contact planarization equipment and materials.

Brewer Science creates value through innovative technologies.

Contacts for EMC^{3D} Members include:

Equipment Members:

Alcatel, France; (Paris: CGEP.PA and NYSE: ALA) Jean-Marc Gruffat, Director of Business Development

Technology: Si and dielectric etching using DRIE

EV Group, Austria; Thorsten Matthias, Director of Technology North America

Technology: bonding, thin wafer handling, mask alignment lithography, conformal coat and develop

SEMITOOL Inc, USA; (Nasdaq: SMTL), Bioh Kim, Director of 3D Interconnect

Technology: electroplating, metal/barrier etch, photoresist strip, wafer cleaning and thinning

XSiL Ltd, Ireland; Richard F. Toftness, Vice President of Business Development

Technology: Si laser machining, via drilling, and wafer dicing

Isonics Corp, USA; (NASDAQ: ISON) Kim Bell, Director of Sales

Technology: wafer service (reclaim and test wafers, wafer thinning, and thick-film SOI wafers)

Materials Members:

AZ Electronic Materials, USA; Aldo Orsi, Global Product Manager

Technology: positive and negative acting photoresists

Enthone (Cookson Electronics), USA; Kristian Story, Key Account and Regional Line Manager

Technology: chemistry for electroplating and metal etch

Honeywell Electronic Materials, USA; (NYSE: HON) Brian Larabee, Strategic Marketing Director

Technology: thermal spreaders, thermal interface materials, and electrical interconnect products

Rohm and Haas, USA; Bob Forman, Advanced Packaging Business Manager

Technology: chemistry for lithography, plating, etching, dielectric formation, and bonding

Brewer Science, Inc., USA; Laura Mauer, Associate Director of R&D Advanced Technologies

Technology: Materials used in litho, wafer thinning, wafer etching and anti-reflective coatings as well as spin-coat/develop/bake equipment.

Technology Members:

Fraunhofer IZM, Germany; Jürgen Wolf, Group and Project Manager

KAIST (Korea Advanced Institute of Science and Technology), Korea; Dr. Kyung-Wook Paik, Professor

SAIT (Samsung Advanced Institute of Technology), Korea; Dr. Yoon-Chul Sohn, Researcher

TAMU (Texas A&M University), USA; Dr. Manuel Soriaga, Professor