

TSV 3-D Packaging on Track for 2008

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According to the [2006 International Technology Roadmap for Semiconductors](#) (ITRS), interconnect schemes represent one of the key next-generation manufacturing challenges due to variability associated with, among other things, trench and via depth and profile, as well as thinning caused by cleaning and chemical mechanical planarization (CMP). The ITRS goes on to state that “traditional interconnect scaling will no longer satisfy performance requirements. Defining and finding solutions beyond copper and low-k will require...accelerated design, packaging and unconventional interconnect.”

This illustrates why through-silicon vias (TSVs) for 3-D packaging applications have now become a hot topic in their own right — and why Alcatel, EV Group, Semitool and XSiL joined forces just over a year ago to launch the [EMC-3D Consortium](#). Formed to create and help drive implementation of a cost-effective TSV process for chip stacking and packaging of MEMS/sensors, EMC-3D has met its first-year objectives, thanks to the contributions of its 14 equipment, materials and R&D members spanning Europe, Asia and North America. The latest addition to the consortium’s roster, Brewer Science, brings its expertise in specialty materials — specifically, high-temperature temporary adhesives.

In the past year, consortium representatives met with more than 1000 high-level attendees. From the enthusiastic response, it was clear that EMC-3D is on the right track with its three-year program, as device manufacturers increasingly recognize the cost and performance advantages associated with TSVs. More than 16 companies already have equipment from the consortium running in R&D or pilot lines, according to equipment members. Based on this early strong showing, it is expected that copper TSV will rapidly become an adopted interconnect process.

The consortium’s first-year goal was to demonstrate its via-first TSV process flow for 200 mm wafers; in fact, the first completed wafers from the member companies’ virtual line are expected by the end of 2007. Even more significant, we’re seeing that the first customers actually plan to bring the TSV process into production in 2008, with initial products incorporating TSVs going to market later in the year. It’s expected that memory and specialty product makers will be the first users, closely followed by logic providers.

Sophomore year brings new challenges

In 2008, the consortium will still be working on 200 mm wafers, but its main goal will be to further stabilize the process, increasing throughput and reducing equipment cost. In addition, thinner wafers will be used, enabling the creation of shorter, smaller-diameter vias with lower aspect ratios to bring costs down even further for both via-first and via-last TSV processes. (Note: EMC-3D refers to “via-first” as via creation before the wafer is thinned and “via-last” as post-thinning via creation.) While 300 mm work is slated to start in the third year, customers are clamoring for acceleration of this timeline, particularly in the memory sector. This may be viable, as all member companies will become capable of 300 mm in the next calendar year.

It’s important to note that, unlike some collaborative entities, EMC-3D is not creating a bundled process flow for licensing, and the consortium owns no IP. Member companies retain ownership of their own IP for each piece of the flow. End users can select the process modules they need, or, if they want to invest in the entire flow, they can secure process transfer from the member companies individually. This non-ownership of collective IP by EMC-3D creates an open structure, giving end users the freedom to work with preferred suppliers for lithography, electroplating, deep reactive ion etch (DRIE), laser drilling, bonding and other steps where long-term partnerships exist.

Looking to the future

By the end of its third year, EMC-3D seeks to reduce overall cost of ownership (CoO) for the TSV virtual process flow to <\$200/wafer. This CoO target, established through collaboration with experts from throughout the packaging industry, would make TSV competitive with existing packaging technology while delivering significant form-factor and performance improvements. Thus, we see the end of the decade as the inflection point at which TSV becomes the new standard for memory packaging, DRAM and flash, while the beginning of the next decade will see the first examples of TSV integrated devices.