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EMC-3D

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Datacon Technology joins EMC-3D consortium to develop cost-effective 3D Thru-Silicon-Via interconnects

Die bonding & sorting equipment manufacturer Datacon joins EMC-3D to provide high-precision assembly expertise to the Thru-Silicon-Via (TSV) international consortium.

Radfield, Austria -April 8, 2008. The international semiconductor equipment and materials consortium EMC^{3D} today announced that Datacon Technology has joined the organization. EMC^{3D} is dedicated to providing cost-effective integrated Thru-Silicon-Via (TSV) technology for chip stacking applications.

EMC-3D is addressing the technical, integration and economic issues of creating 3-D interconnects using TSV technology for chip stacking and advanced MEMS/sensors packaging. Through collaboration with research partners, the consortium will develop unit processes for creating micro-vias between 5 and 30 μm on 50 μm thinned 200mm and 300mm wafers using via-first and die-to-wafer techniques. The primary goals of the consortium are to create a robust integrated process flow at a cost of less than \$200USD per wafer.

Datacon provides die bonding and sorting equipment used in advanced assembly by the semiconductor and telecommunications industries. One of the key integration issues in 3D interconnect is the efficiency and accuracy of the die-to-wafer attach for both TSV and MEMS/sensor applications.

“One of the challenging integration issues of TSV is the die-to-wafer bonding and the cost associated with this step,” said Markus Wimplinger, EMC^{3D} board member and director of business unit technology development at EV Group. “Datacon will bring a significant expertise needed to achieve the aggressive goals of the EMC^{3D} consortium.”

About Datacon

Datacon Technology GmbH is a leading global manufacturer of die bonding & sorting equipment for the semiconductor, telecommunication and automotive industries. Datacon was founded in 1986 and since the beginning of 2005 has been part of the Dutch Besi group (BE Semiconductor Industries N.V.), an international group of companies operating in the semiconductor industry. Datacon's primary expertise is the development and production of high-precision assembly equipment for the advanced packaging market.

About EMC-3D (or EMC3D)

EMC3D (Semiconductor 3D Equipment and Materials Consortium) was created in October 2006 to develop a new 3D market and technology by demonstrating a cost-effective, manufacturable, stackable TSV interconnection process for IC and MEMS/Sensor packaging.

www.EMC3D.org

Contacts for EMC^{3D} Members include:

Equipment Members:

Alcatel, France; (Paris: CGEP.PA and NYSE: ALA) Jean-Marc Gruffat, Director of Business Development
Technology: Si and dielectric etching using DRIE
Datacon Technology GmbH, Austria; Christoph Scheiring, Director Product Marketing
Technology: Precision Diebonding & Sorting
EV Group, Austria; Thorsten Matthias, Director of Technology North America
Technology: bonding, thin wafer handling, mask alignment lithography, conformal coat and develop
SEMITOOL Inc, USA; (NASDAQ: SMTL), Rozalia Beica, 3D Business and Technology Director
Technology: electroplating, DOB, metal/barrier etch, photoresist strip, wafer cleaning and thinning
XSiL Ltd, Ireland; Dr. Alexey Rodin, Via Team Leader
Technology: Si laser machining, via drilling, and wafer dicing
Isonics Corp, USA; (NASDAQ: ISON) Joanna Lohkamp, General Manager
Technology: wafer service (reclaim and test wafers, wafer thinning, and thick-film SOI wafers)

Materials Members:

AZ Electronic Materials, USA; Aldo Orsi, Global Product Manager
Technology: positive and negative acting photoresists
Brewer Science, Inc., USA; Laura Mauer, Associate Director of R&D Advanced Technologies
Technology: Materials used in litho, wafer thinning, wafer etching and anti-reflective coatings as well as spin-coat/develop/bake equipment.
Enthone (Cookson Electronics), USA; Yun Zhang, Director, Research and Development
Technology: chemistry for electroplating and metal etch
Rohm and Haas, USA; Bob Forman, Advanced Packaging Business Manager
Technology: chemistry for lithography, plating, etching, dielectric formation, and bonding

Technology Members:

CEA-LETI, Grenoble France; Mark Scannell, Microelectronics Program Manager
Fraunhofer IZM, Germany; Jürgen Wolf, Group and Project Manager
KAIST (Korea Advanced Institute of Science and Technology), Korea; Dr. Kyung-Wook Paik, Professor
NXP, Dr. Fred Roozeboom, Technical Advisor
SAIT (Samsung Advanced Institute of Technology), Korea; Dr. Yoon-Chul Sohn, Researcher
TAMU (Texas A&M University), USA; Dr. Manuel Soriaga, Professor